REMARKS

The present application was filed on May 25, 2001 with claims 1 through 35. Claims 1 through 35 are presently pending in the above-identified patent application.

In the Office Action, the Examiner objected to the title of the invention for not being descriptive. The Examiner provisionally rejected claims 1-26 under the judicially created doctrine of double patenting as being unpatentable over claims 1-28 of copending Application No. 10/060661. The Examiner rejected claims 1-5, 9-14, 17, 20, 21, 23, and 24 under 35 U.S.C. §103(a) as being unpatentable over Sherlock et al. (United States Patent Number 6,157,977), in view of Fuller (United States Patent Number 5,632,038), rejected claims 15, 16, 25, and 26 under 35 U.S.C. §103(a) as being unpatentable over Sherlock et al. in view of Fuller and Takahashi (United States Patent Number 6,345,336), and rejected claims 27-29 and 31-35 under 35 U.S.C. §103(a) as being unpatentable over Sherlock et al., in view of Stein et al., Session V: "Storage Array and Sense/Refresh Circuit for Single-Transistor Memory Cells," 1972, pages 56-57, and Fuller. The Examiner indicated that claims 6-8, 18, 19, 22, and 30 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

The present invention is directed to a method and apparatus for reducing leakage power in a cache memory. A cache decay technique is employed for both data and instruction caches that removes power from cache lines that have not been accessed for a predefined time interval, referred to as the decay interval. The cache-line granularity of the present invention permits a significant reduction in leakage power while at the same time preserving much of the performance of the cache. The decay interval is maintained using a timer that is reset each time the corresponding cache line is accessed. The decay interval may be fixed or variable. Once the decay interval timer exceeds a specified decay interval, power to the cache line is removed. Once power to the cache line is removed, the contents of the data and tag fields are allowed to decay and the valid bit associated with the cache line is reset. When a cache line is later accessed after being powered down by the present invention, a cache miss is incurred while the cache line is again powered up and the data is obtained from the next level of the memory hierarchy.

The specification has been amended to correct a typographical error.

Formal Objections

The title of the invention was objected to for not being descriptive. The title has been amended to be more descriptive. Applicants respectfully request that the objection to the title be withdrawn.

Double Patenting Rejection

Claims 1-26 were provisionally rejected under the judicially created doctrine of double patenting as being unpatentable over claims 1-28 of copending Application No. 10/060,661. In particular, the Examiner asserts that the referenced co-pending application and the instant application are claiming common subject matter, as follows: "removes power said associated cache line after a decay interval." The Examiner further asserts that there is no apparent reason why Applicants would be prevented from presenting claims corresponding to those of the instant application in the other co-pending application.

Applicants submit that the Double Patenting rejection is improper in the present earlier filed application. The present application will necessarily expire before the expiration date of the later filed copending Application No. 10/060,661. In the Office Action, the Examiner asserts that there is "no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application." Applicants, note, however, that the current claims are fully supported by the current specification and are entitled to the earlier priority date provided by the present application.

Applicants thus respectfully request reconsideration and withdrawal of the provisional rejection under the judicially created doctrine of double patenting.

Independent Claims 1, 20, 27 and 34

Independent claims 1 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sherlock et al., in view of Fuller, and claims 27 and 34 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sherlock et al., in view of Stein et al. and Fuller.

Regarding claim 1, the Examiner acknowledges that Sherlock does not explicitly teach "using the timer configured to control signal that removes power to said

associated cache line after a decay interval," but asserts that Fuller teaches this limitation.

First, Applicants note that the "timer" taught by Sherlock does not measure a decay interval, as required by independent claim 1. Sherlock actually teaches away from the present invention by teaching that the "timer" (CLA 58) "measures the age of the data held in an associated cache line in units of elapsed PIO write acceptances" (col. 5, lines 19-21), and is reset each time data is fetched from the associated cache line. The timer does ***not*** measure a *decay interval.*

Second, Applicants note that, in the text cited by the Examiner, Fuller teaches that "the control and power management logic monitors the activity of the processor and automatically places the secondary cache memory into a low power mode (such as, for example, turning off the cache) during periods of inactivity." (Col. 3, lines 18-22.) Thus, Fuller teaches to turn off the *entire secondary cache* (*not a line of the cache*). Independent claim 1 requires a timer associated with *each of said plurality of cache lines*, each of said timers configured to control a signal that *removes power to said associated cache line* after a decay interval. Independent claim 20 requires resetting said timer each time said cache line is accessed; and *removing power from said associated cache line* after a decay interval.

In addition, Fuller actually teaches away from the present invention by teaching to base the decision to turn off the cache based on the *inactivity of the processor* (col. 3, lines 22-30). Independent claims 1 and 20 require removing power from an associated cache line *after a decay interval.*

Thus, Sherlock et al. and Fuller, alone or in any combination, do not disclose or suggest a timer associated with each of said plurality of cache lines, each of said timers configured to control a signal that removes power to said associated cache line after a decay interval, as required by independent claim 1, and do not disclose or suggest resetting said timer each time said cache line is accessed; and removing power from said associated cache line after a decay interval, as required by independent claim 20.

Regarding claim 27, the Examiner asserts that Sherlock discloses a timer associated with each of said plurality of cache lines, each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period.

First, Applicants could find no disclosure in Sherlock of *resetting a valid bit* associated with the cache line after a safe period. The CLA 58 cited by the Examiner is a counter, not a valid bit, and "is reset to zero each time data is fetched..." (Col. 5, lines 11-15.)

Second, as noted above, Sherlock teaches that the timer (CLA 58) "measures the age of the data held in an associated cache line in units of elapsed PIO write acceptances" (col. 5, lines 19-21), and is reset each time data is fetched from the associated cache line. The timer does ***not*** measure the period of time during which *DRAM cells reliably store a value,* as defined in the context of the present invention and as is well known in the art. Independent claim 27 requires that each of said timers controls a "signal that resets a valid bit associated with said cache line after said *safe period.*" Independent claim 34 requires "resetting a valid bit associated with said cache line after said *safe period.*" The safe period in the present invention is defined in independent claims 27 and 34 as the period of time during which the *DRAM cells reliably store a value.*

Thus, Sherlock does not disclose or suggest that "each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period," as required by independent claim 27, and does not disclose or suggest "resetting a valid bit associated with said cache line after said safe period," as required by independent claim 34.

Additional Cited References

Takahashi was also cited by the Examiner for its disclosure of a "first access to a cache line that has been powered down results in a cache miss, resets said corresponding timer and restores power to said cache line." Applicants note that Takahashi is directed to a method for reducing power consumption in the tag RAM of an instruction cache memory. (See, Abstract.) Takahashi, however, does not address the issue of timers associated with cache lines.

Thus, Takahashi does not disclose or suggest a timer associated with each of said plurality of cache lines, each of said timers configured to control a signal that removes power to said associated cache line after a decay interval, as required by independent claim 1, does not disclose or suggest resetting said timer each time said

cache line is accessed; and removing power from said associated cache line after a decay interval, as required by independent claim 20, does not disclose or suggest that each of said timers controls a signal that resets a valid bit associated with said cache line after said safe period, as required by independent claim 27, and does not disclose or suggest resetting a valid bit associated with said cache line after said safe period, as required by independent claim 34.

Stein et al. was also cited by the Examiner for its disclosure of one or more dynamic random memory access (DRAM) cells. Stein et al., however, do not address the issue of timers associated with cache lines.

Thus, Stein et al. do not disclose or suggest a timer associated with each of said plurality of cache lines, each of said timers configured to control a signal that removes power to said associated cache line after a decay interval, as required by independent claim 1, do not disclose or suggest resetting said timer each time said cache line is accessed; and removing power from said associated cache line after a decay interval, as required by independent claim 20, do not disclose or suggest that each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period, as required by independent claim 27, and do not disclose or suggest resetting a valid bit associated with said cache line after said safe period, as required by independent claim 34.

Dependent Claims 2-19, 21-26, 28-33 and 35

Dependent claims 2-5, 9-14, 17, 21, 23, and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sherlock et al., in view of Fuller, claims 15, 16, 25, and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sherlock et al. in view of Fuller and Takahashi, and claims 28-29, 31-33, and 35 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sherlock et al., in view of Stein et al. and Fuller.

Claims 2-19, 21-26, 28-33 and 35 are dependent on claims 1, 20, 27, and 34, respectively, and are therefore patentably distinguished over Sherlock et al., Fuller, Takahashi, and Stein et al. (alone or in any combination) because of their dependency from independent claims 1, 20, 27, and 34 for the reasons set forth above, as well as other elements these claims add in combination to their base claim. The Examiner has already

indicated that claims 6-8, 18, 19, 22, and 30 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

All of the pending claims, i.e., claims 1-35, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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